



ACE1357B

P-Channel Enhancement Mode Field Effect Transistor

Description

These P-Channel enhancement mode field effect transistors are produced using high cell density, DMOS technology.

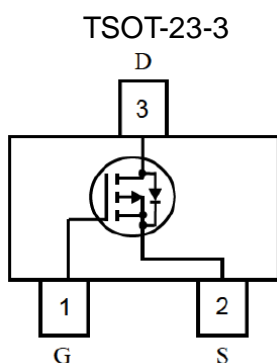
Features

- $V_{DS} (V) = -20V, I_D = -2A (V_{GS} = -4.5V)$
- $R_{DS(ON)} < 120m\Omega @ V_{GS} = -4.5V$
- $R_{DS(ON)} < 150m\Omega @ V_{GS} = -2.5V$
- TSOT-23-3 Package

Absolute Maximum Ratings

Parameter	Symbol	Max	Unit
Drain-Source Voltage	V_{DSS}	-20	V
Gate-Source Voltage	V_{GSS}	± 12	V
Drain Current (Continuous)	I_D	$T_A = 25^\circ C$	-2
		$T_A = 70^\circ C$	-1.8
Drain Current (Pulsed)	I_{DM}	-7	A
Power Dissipation	$T_A = 25^\circ C$	P_D	1
Operating temperature / storage temperature	T_J / T_{STG}	-55~150	$^\circ C$

Packaging Type



Ordering information

ACE1357B XXX + H

- └─ Halogen - free
- └─ Pb - free
- └─ BMS: TSOT-23-3



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Electrical Characteristics

$T_A=25^{\circ}\text{C}$, unless otherwise specified.

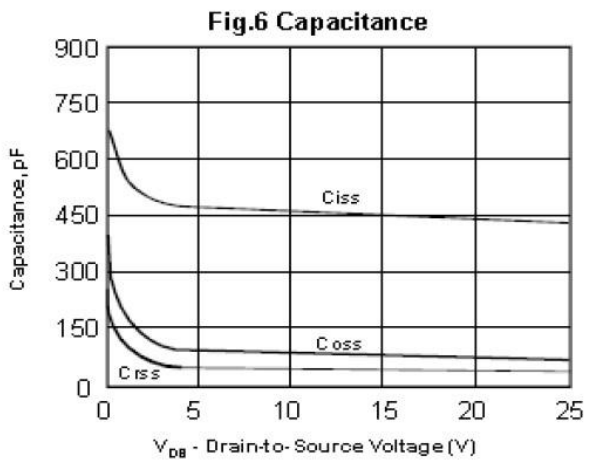
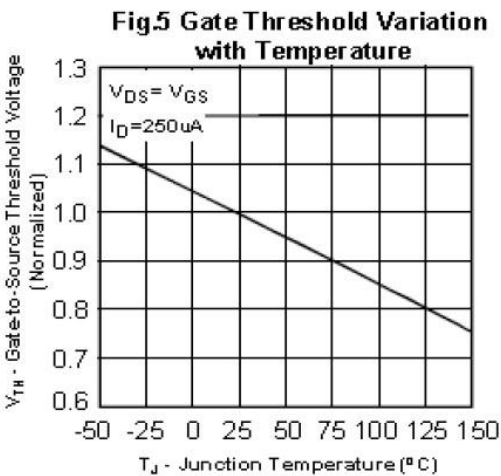
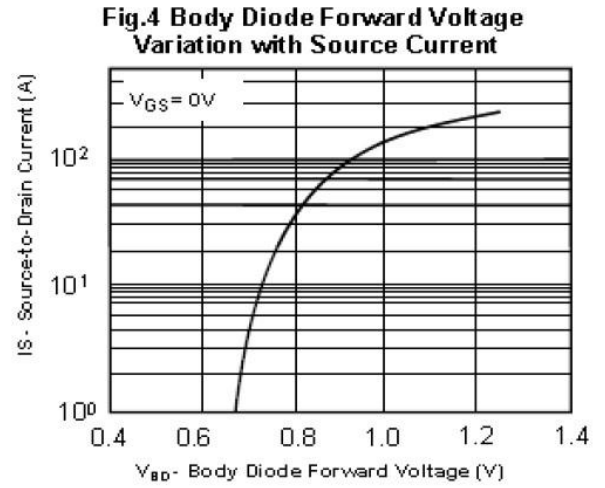
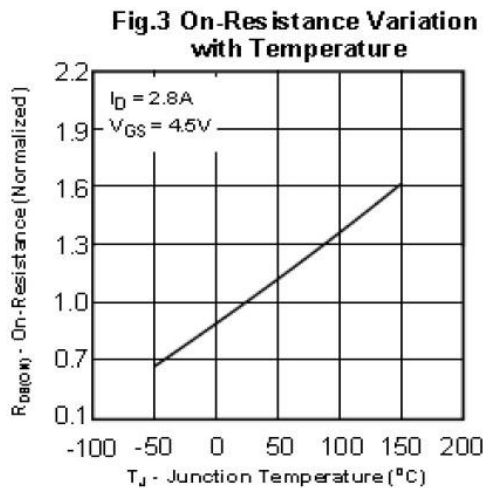
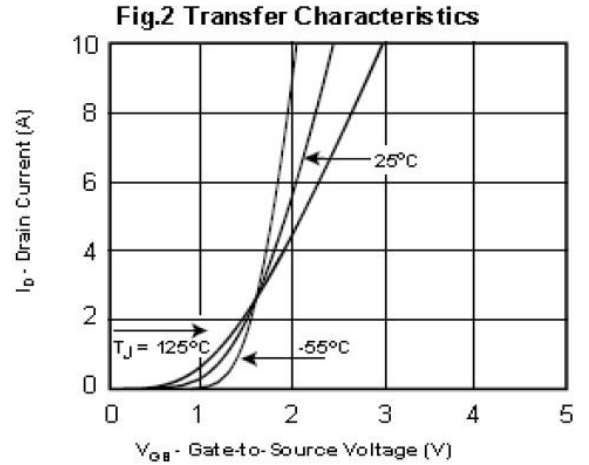
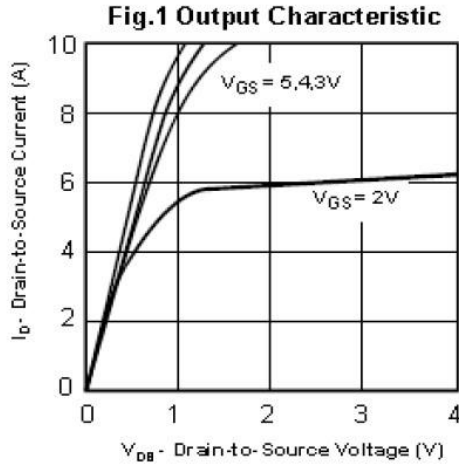
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Static						
Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=-250\mu A$	-20			V
Zero gate voltage drain current	I_{DSS}	$V_{DS}=-20V, V_{GS}=0V$			-1	μA
Gate threshold voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}, I_{DS}=-250\mu A$	-0.4	-0.65	-0.9	V
Gate leakage current	I_{GSS}	$V_{GS}=\pm 12V, V_{DS}=0V$			± 100	nA
Drain-source on-state resistance	$R_{DS(ON)}$	$V_{GS}=-4.5V, I_D=-2A$		88	120	m Ω
		$V_{GS}=-2.5V, I_D=-1A$		120	150	
Forward trans conductance	g_{FS}	$V_{DS}=-5V, I_D=-2.8A$		6.5		S
Diode forward voltage	V_{SD}	$I_{SD}=-1.6A, V_{GS}=0V$		-0.86	-1.1	V
Max Diode Forward Voltage	I_S				-1.6	A
Switching						
Total gate charge	Qg	$V_{GS}=-4.5V, V_{DS}=-6V, I_D=-2.8A$		4.9		nC
Gate-source charge	Qgs			0.62		
Gate-drain charge	Qgd			1.07		
Turn-on delay time	$t_{d(on)}$	$V_{DD}=-6V, R_L=6\Omega, I_D=-1A,$ $V_{GEN} = -4.5V R_G = 6\Omega$		10.1		ns
Turn-on rise time	Tr			4.76		
Turn-off delay time	$t_{d(off)}$			84.1		
Turn-off fall time	Tf			25.2		
Dynamic						
Input capacitance	Ciss	$V_{GS}=0V, V_{DS}=-6V, f=1.0MHz$		472		pF
Output capacitance	Coss			71		
Reverse transfer capacitance	Crss			51		

Notes:

1. Pulse width limited by maximum junction temperature.
2. Pulse test: $PW \leq 300\mu s$, duty cycle $\leq 2\%$.
3. For design AID only, not subject to production testing.
4. Switching time is essentially independent of operating temperature.



Typical Performance Characteristics





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Fig. 7 Gate Charge Waveform

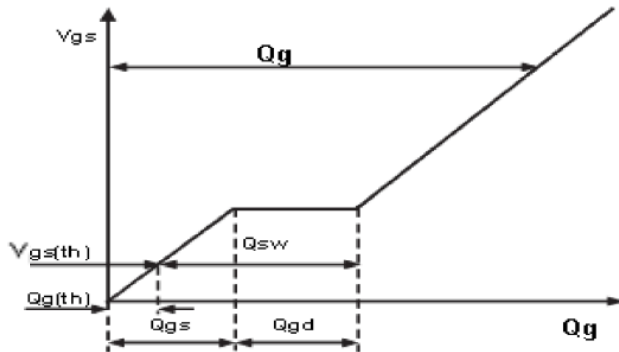


Fig. 8 Gate Charge

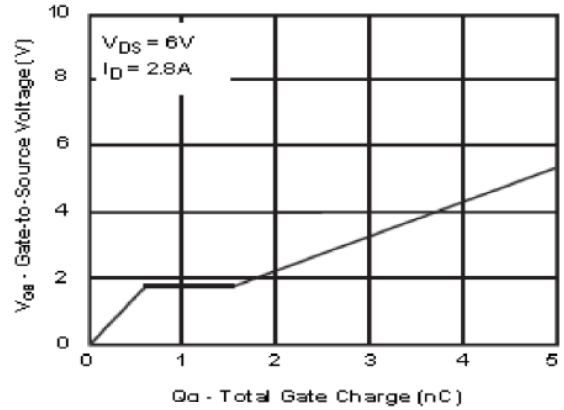


Fig. 9 Maximum Safe Operating Area

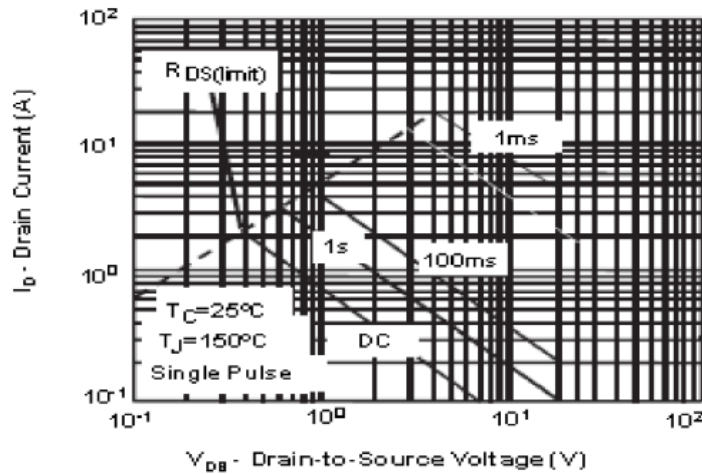
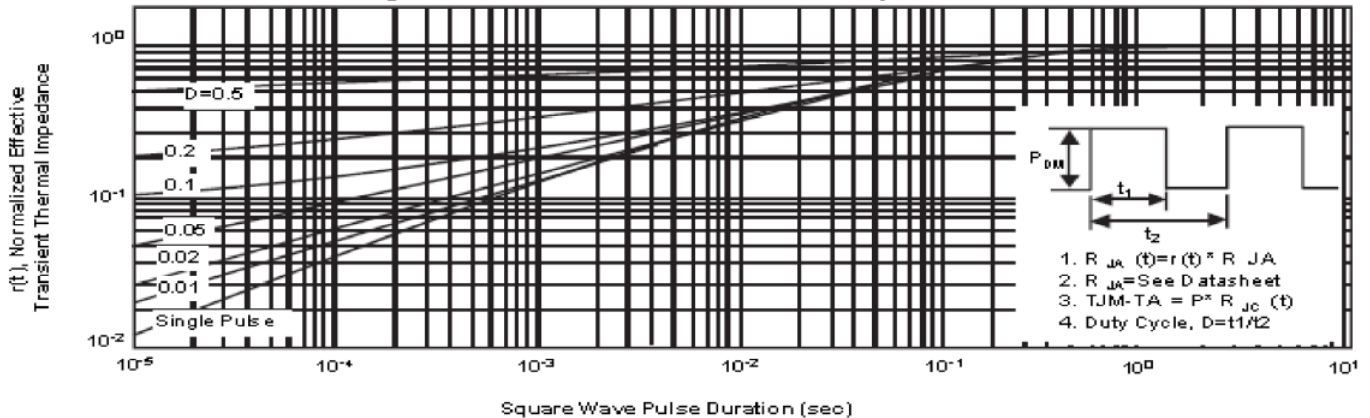


Fig. 10 Normalized Thermal Transient Impedance Curve

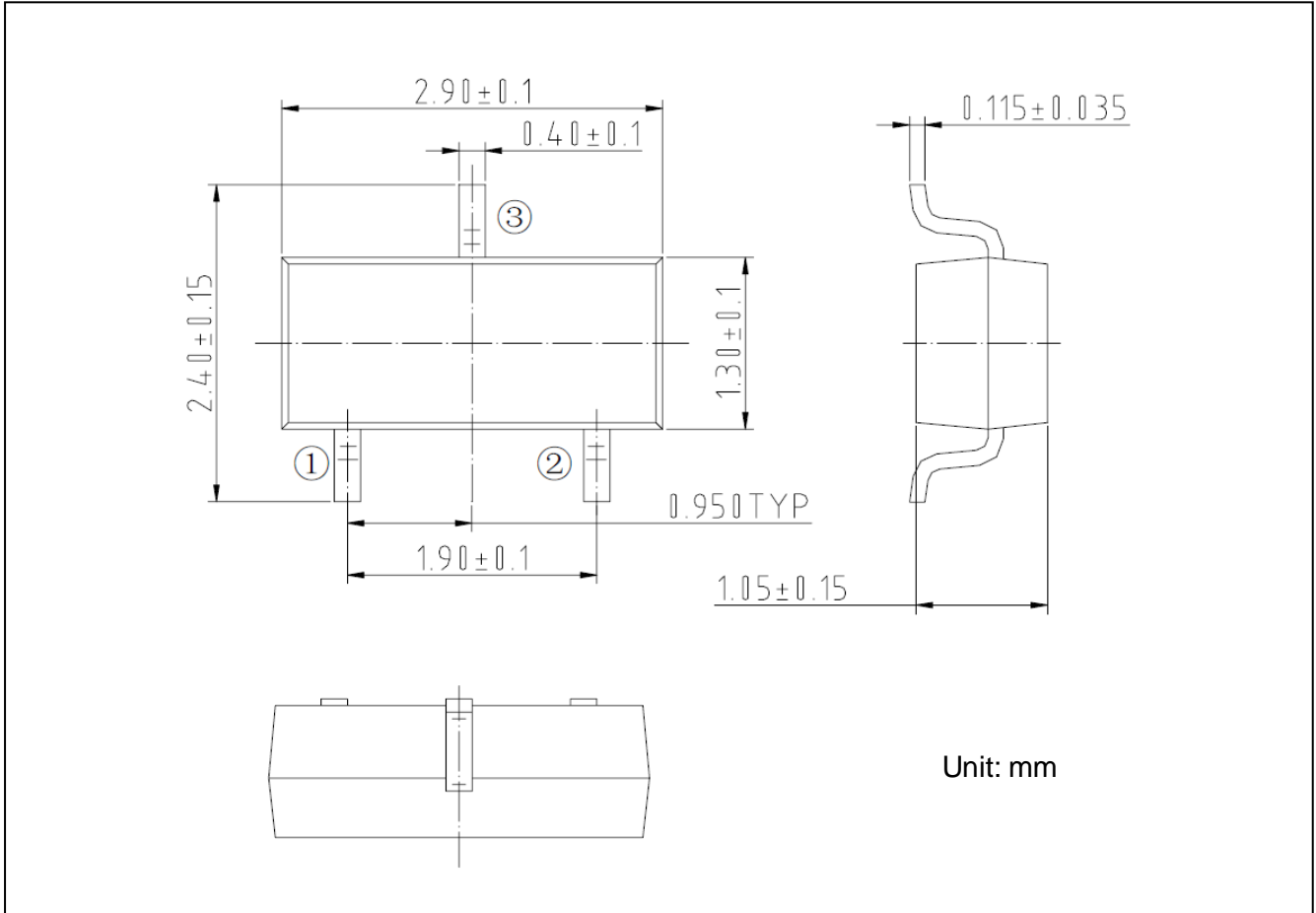




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Packing Information

TSOT-23-3





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Notes

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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