



ACE14422B

N-Channel Enhancement Mode Power MOSFET

Description

ACE14422B uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

Features

- $V_{DS} (V) = 20V, I_D = 55A$
- $R_{DS(ON)} @ V_{GS} = 10V, TYP 2.4m\Omega$
- $R_{DS(ON)} @ V_{GS} = 4.5V, TYP 2.6m\Omega$
- $R_{DS(ON)} @ V_{GS} = 2.5V, TYP 3.5m\Omega$

Absolute Maximum Ratings

| Parameter | Symbol | Max | Unit |
|---|----------------|-------------------|------------|
| Drain-Source Voltage | V_{DSS} | 20 | V |
| Gate-Source Voltage | V_{GSS} | ± 12 | V |
| Drain Current (Continuous) ^{*AC} | I_D | $T_A=25^\circ C$ | 55 |
| | | $T_A=100^\circ C$ | 42 |
| Drain Current (Pulse) ^{*B} | I_{DM} | 180 | A |
| Power Dissipation | P_D | 78 | W |
| Operating and Storage Temperature Range | T_J, T_{STG} | -55 to 150 | $^\circ C$ |

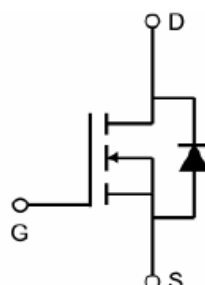
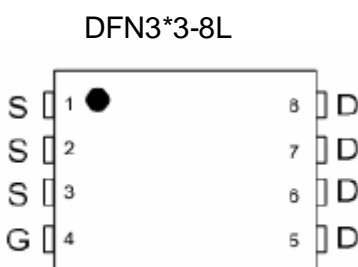
A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ C$. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ and the maximum allowed junction temperature of $150^\circ C$. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on $T_{J(MAX)}=150^\circ C$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}=150^\circ C$. Ratings are based on low frequency and duty cycles to keep initial $T_J = 25^\circ C$.

D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.

Packaging Type



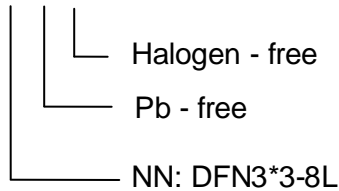


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Ordering information

ACE14422B XX + H



Electrical Characteristics $T_A=25\text{ }^\circ\text{C}$ unless otherwise noted

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|-----------------------------------|---------------|--|------|------|-----------|------------|
| Static | | | | | | |
| Drain-Source Breakdown Voltage | $V_{(BR)DSS}$ | $V_{GS}=0V, I_D=250\mu A$ | 20 | | | V |
| Zero Gate Voltage Drain Current | I_{DSS} | $V_{DS}=20V, V_{GS}=0V$ | | | 1 | μA |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS}=V_{GS}, I_{DS}=250\mu A$ | 0.4 | 0.75 | 1.5 | V |
| Gate Leakage Current | I_{GSS} | $V_{GS}=\pm 12V, V_{DS}=0V$ | | | ± 100 | nA |
| Static Drain-Source On-Resistance | $R_{DS(on)}$ | $V_{GS}=10V, I_D=20A$ | | 2.4 | 3 | m Ω |
| | | $V_{GS}=4.5V, I_D=15A$ | | 2.6 | 3.5 | |
| | | $V_{GS}=2.5V, I_D=7A$ | | 3.5 | 5 | |
| Forward Transconductance | g_{FS} | $V_{DS}=5V, I_D=10A$ | 85 | | | S |
| Diode Forward Voltage | V_{SD} | $I_{SD}=1A, V_{GS}=0V$ | | | 1 | V |
| Diode Forward Current | I_S | | | | 40 | A |
| Switching | | | | | | |
| Total Gate Charge | Q_g | $V_{DS}=10V, I_D=10A$ $V_{GS}=10V$ | | 72 | | nC |
| Gate-Source Charge | Q_{gs} | | | 6.5 | | |
| Gate-Drain Charge | Q_{gd} | | | 8.5 | | |
| Turn-On Delay Time | $T_{d(on)}$ | $V_{DD}=10V, V_{GS}=10V$ $R_{GEN}=3\Omega, I_D=1\Omega$ | | 8 | | ns |
| Turn-On Rise Time | t_f | | | 11 | | |
| Turn-Off Delay Time | $t_{d(off)}$ | | | 62 | | |
| Turn-Off Fall Time | t_f | | | 23 | | |
| Dynamic | | | | | | |
| Input Capacitance | C_{iss} | $V_{DS}=10V, V_{GS}=0V$ $f=1.0MHz$ | | 3800 | | pF |
| Output Capacitance | C_{oss} | | | 1430 | | |
| Reverse Transfer Capacitance | C_{rss} | | | 280 | | |



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Typical Performance Characteristics

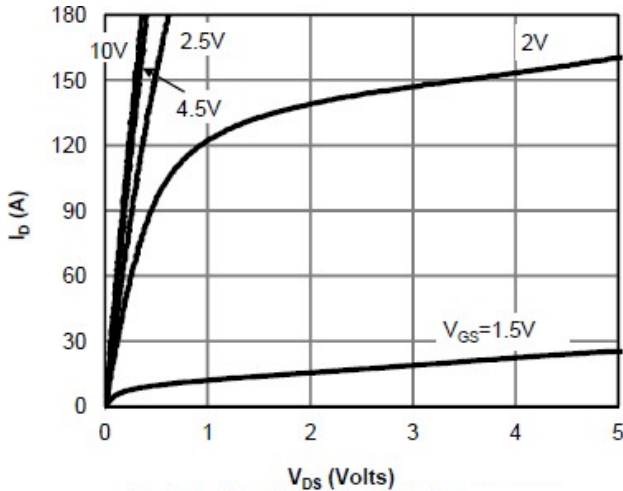


Fig 1: On-Region Characteristics

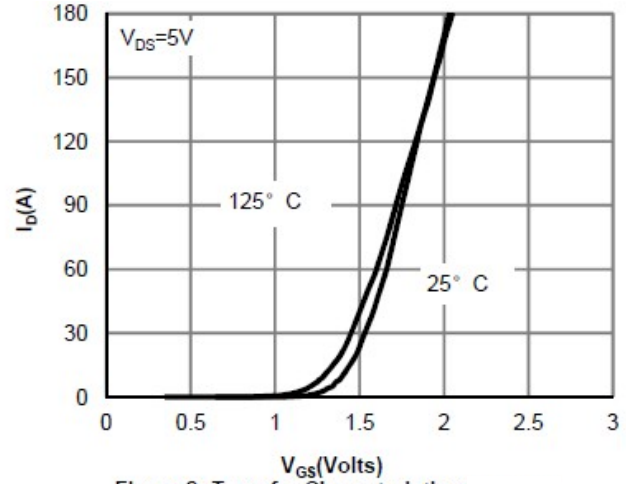


Figure 2: Transfer Characteristics

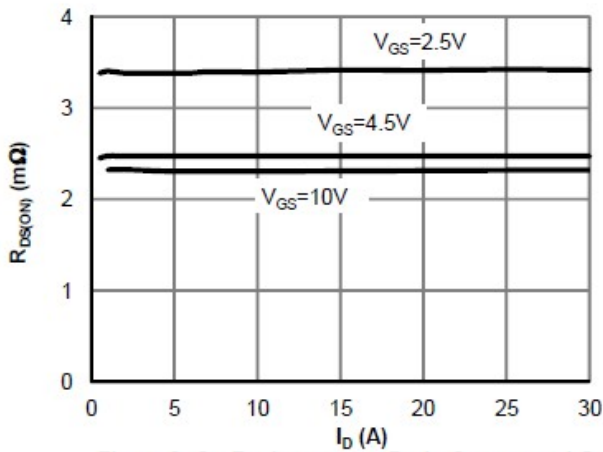


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

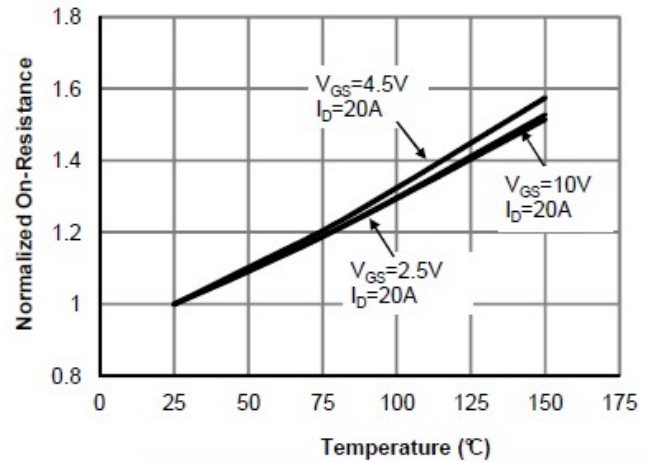


Figure 4: On-Resistance vs. Junction Temperature

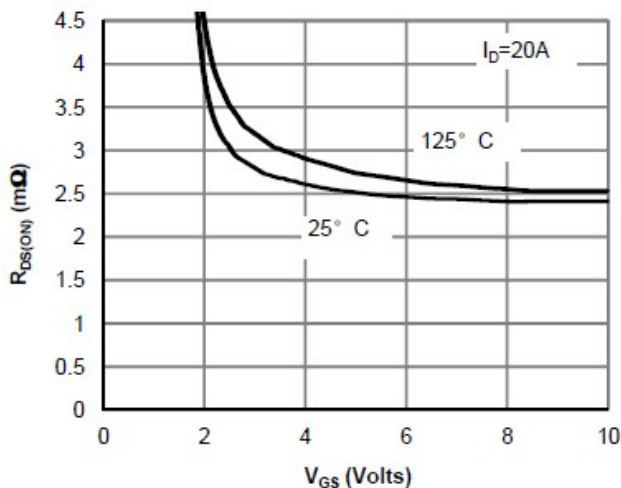


Figure 5: On-Resistance vs. Gate-Source Voltage

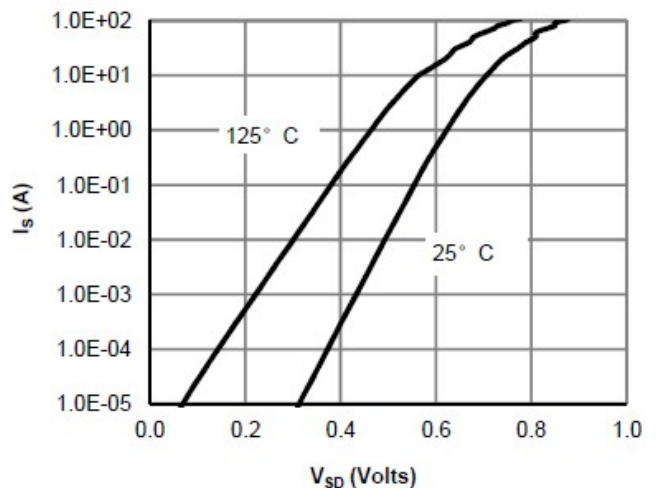


Figure 6: Body-Diode Characteristics



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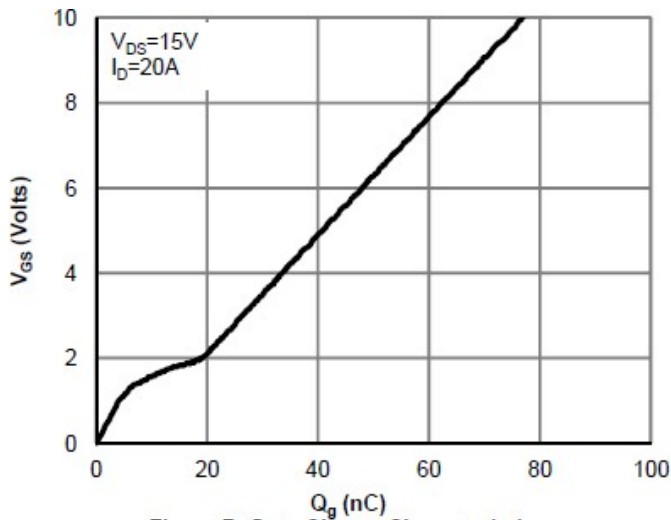


Figure 7: Gate-Charge Characteristics

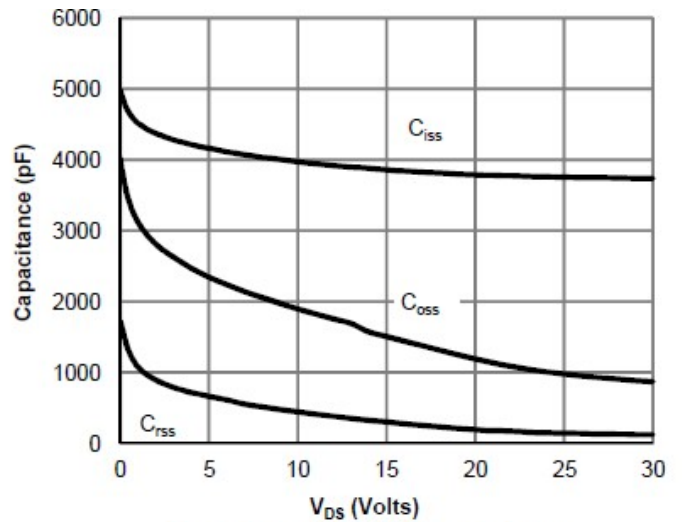


Figure 8: Capacitance Characteristics

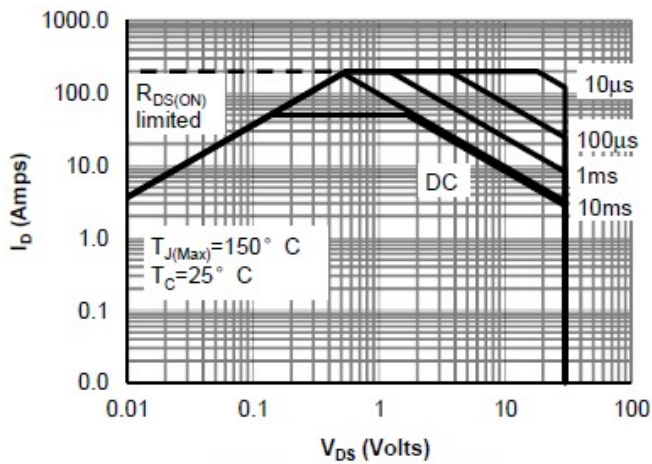


Figure 9: Maximum Forward Biased Safe Operating Area
VGS > or equal to 2.5V

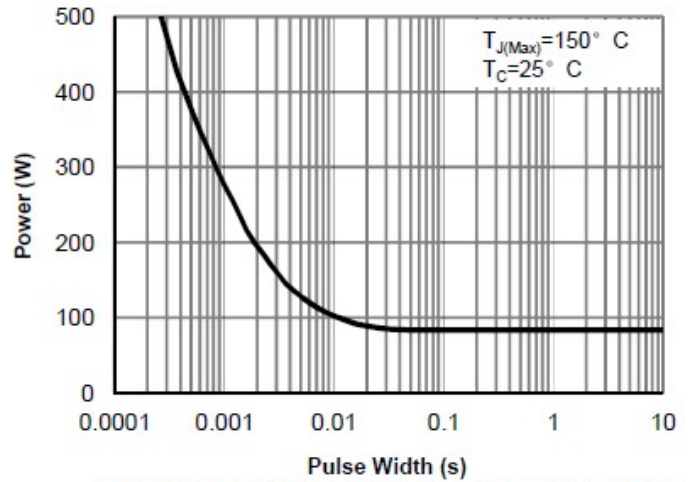


Figure 10: Single Pulse Power Rating Junction-to-Case

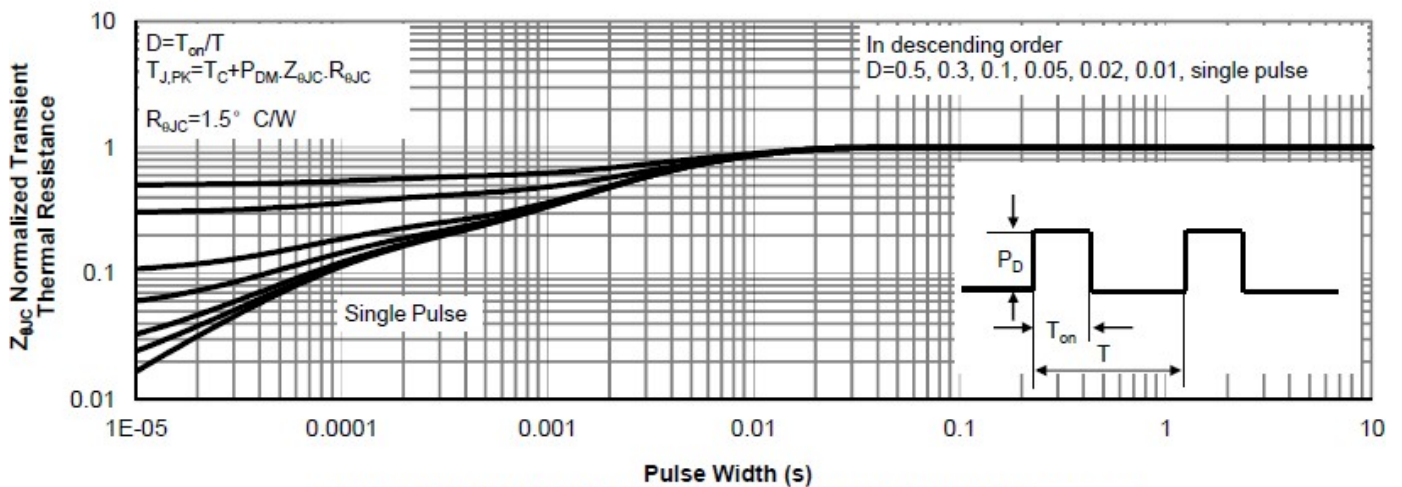


Figure 11: Normalized Maximum Transient Thermal Impedance

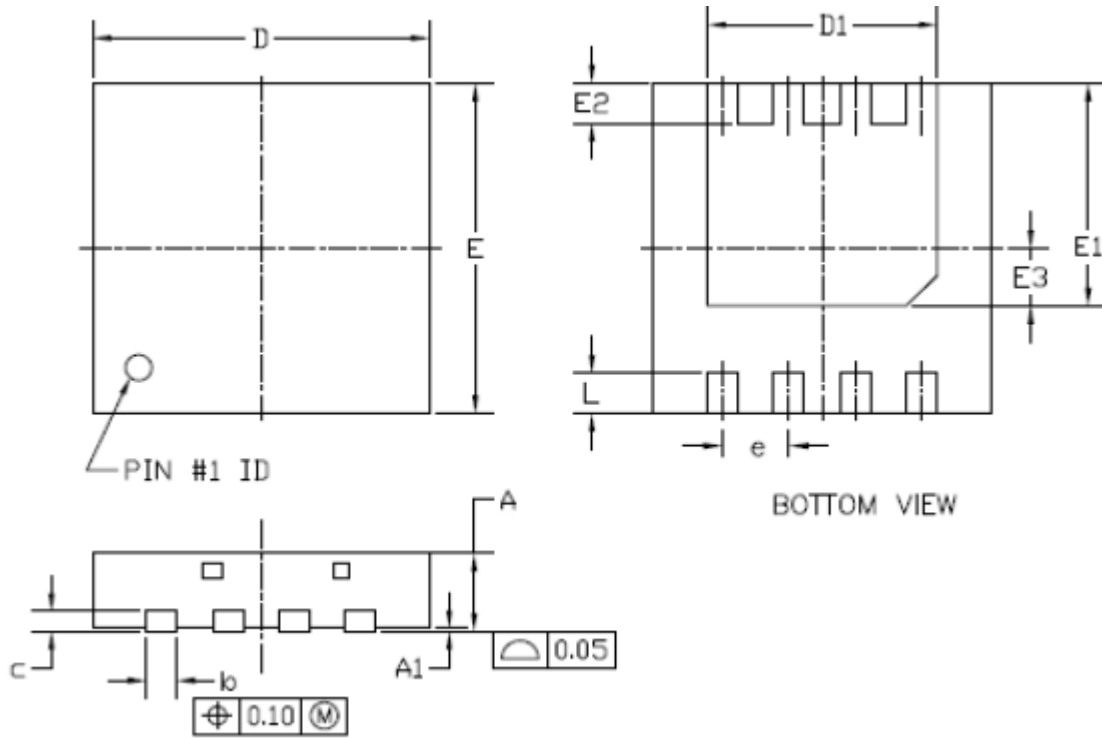


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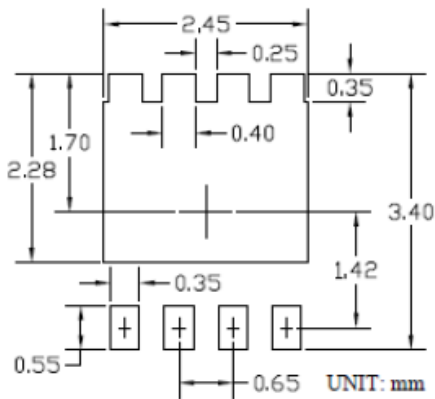
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Packing Information

DFN3*3-8L



RECOMMENDED LAND PATTERN



| SYMBOLS | DIMENSIONS IN MILLIMETERS | | | DIMENSIONS IN INCHES | | |
|---------|---------------------------|------|------|----------------------|-------|-------|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 0.70 | 0.75 | 0.80 | 0.028 | 0.030 | 0.031 |
| A1 | — | — | 0.05 | — | — | 0.002 |
| b | 0.24 | 0.30 | 0.35 | 0.009 | 0.012 | 0.014 |
| c | 0.10 | 0.15 | 0.25 | 0.004 | 0.006 | 0.010 |
| D | 3.20 | 3.30 | 3.40 | 0.126 | 0.130 | 0.134 |
| D1 | 2.15 | 2.25 | 2.35 | 0.085 | 0.089 | 0.093 |
| E | 3.20 | 3.30 | 3.40 | 0.126 | 0.130 | 0.134 |
| E1 | 2.13 | 2.23 | 2.33 | 0.084 | 0.088 | 0.092 |
| E2 | 0.30 | 0.40 | 0.50 | 0.012 | 0.016 | 0.020 |
| E3 | 0.48 | 0.58 | 0.68 | 0.019 | 0.023 | 0.027 |
| e | 0.65 BSC | | | 0.026 BSC | | |
| L | 0.30 | 0.40 | 0.50 | 0.012 | 0.016 | 0.020 |



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Notes

ACE does not assume any responsibility for use as critical components in life support devices or systems without the express written approval of the president and general counsel of ACE Electronics Co., LTD. As sued herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.