ACE16428B

N-Channel Enhancement Mode Field Effect Transistor

Description

The ACE16428B uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge. This device is suitable for use as a high side switch in SMPS and general purpose applications.

Features

- V_{DS} (V) = 30V
- I_D = 40A (V_{GS} = 10V)
- $R_{DS(ON)}$ < 7mΩ (V_{GS} = 10V)
- $R_{DS(ON)}$ < 10.5mΩ (V_{GS} = 4.5V)
- 100% Delta Vsd Tested
- 100% R_g Tested

Absolute Maximum Ratings

Parameter		Symbol	Max	Unit
Drain-Source Voltage		V_{DSS}	30	V
Gate-Source Voltage		V_{GSS}	±20	V
Drain Current (Continuous)	T_A=25°C	I_D	40	A
	T_A=100°C		17	
Drain Current (Pulse) [C]		I_{DM}	50	
Drain Current (Continuous)	T_A=25°C	I_{DSM}	11	A
	T_A=70°C		8	
Power Dissipation [B]	T_A=25°C	P_D	30	W
Operating and Storage Temperature Range		T_J,T_{STG}	-55 to 150	°C
Maximum Junction-to-Ambient [A]	t≦10s	$R_{θJA}$	21	℃/W
Maximum Junction-to-Ambient [A D]	Steady-State		50	℃/W
Maximum Junction-to-Case	Steady-State	$R_{θJC}$	3.5	℃/W

A. The value of $R_{θJA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The Power dissipation P_{DSM} is based on $R_{θJA}$ and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.

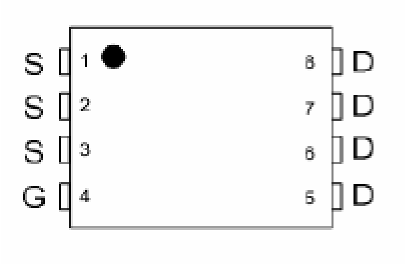
B. The power dissipation P_D is based on $T_{J(MAX)}$=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

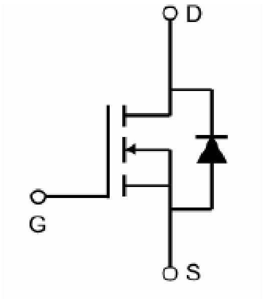
C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150°C. Ratings are based on low frequency and duty cycles to keep initial T_J =25°C.

D. The $R_{θJA}$ is the sum of the thermal impedence from junction to case $R_{θJC}$ and case to ambient.

Packaging Type

DFN5*6-8L-EP





Ordering information

ACE16428B XX + H

- H: Halogen - free
- +: Pb - free
- XX: PN: DFN5*6-8L-EP

Electrical Characteristics T_A=25 °C unless otherwise noted

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D=250uA	30			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=30V, V_{GS}=0V			1	uA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_{DS}=250uA	1	1.6	3	V
Gate Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V			±100	nA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=12A		4.5	7	mΩ
		V_{GS}=4.5V, I_D=10A		6.5	10.5	
Forward Transconductance	g_{FS}	V_{DS}=10V, I_D=12A	30			S
Diode Forward Voltage	V_{SD}	I_{SD}=2A, V_{GS}=0V		0.71	1.0	V
Maximum Body-Diode Continuous Current	I_S				2	A
Switching						
Total Gate Charge	Q_g	V_{DS}=15V, I_D=12A V_{GS}=5V		19		nC
Gate-Source Charge	Q_{gs}			2.7		
Gate-Drain Charge	Q_{gd}			2.5		
Turn-On Delay Time	$T_{d(on)}$	V_{DS}=15V, V_{GS}=10V R_{GEN}=6Ω, R_L=15Ω		10		ns
Turn-On Rise Time	t_f			8		
Turn-Off Delay Time	$t_{d(off)}$			30		
Turn-Off Fall Time	t_f			5		
Dynamic						
Input Capacitance	C_{iss}	V_{DS}=15V, V_{GS}=0V f=1MHz		1625		pF
Output Capacitance	C_{oss}			190		
Reverse Transfer Capacitance	C_{rss}			132		

Note:

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The Power dissipation PDSM is based on $R_{\theta JA}$ and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.

B. The power dissipation PD is based on TJ(MAX)=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150°C. Ratings are based on low frequency and duty cycles to keep initial T_J =25°C.

D. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to case $R_{\theta JC}$ and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedence which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of TJ(MAX)=150°C. The SOA curve provides a single pulse rating.

G. The maximum current rating is package limited.

H. These tests are performed with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C

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Typical Performance Characteristics

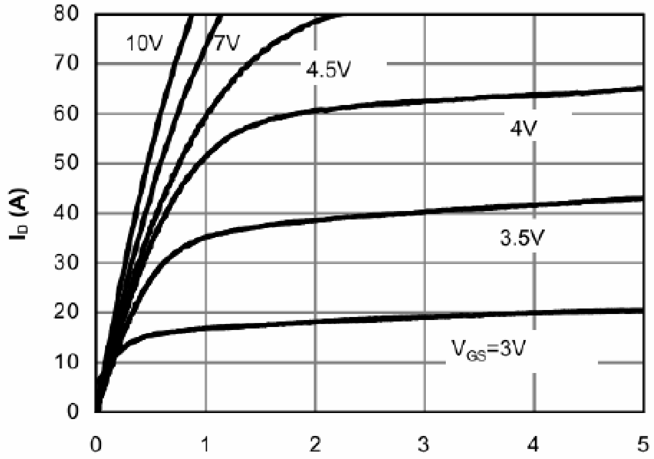


Fig 1: On-Region Characteristics (Note E)

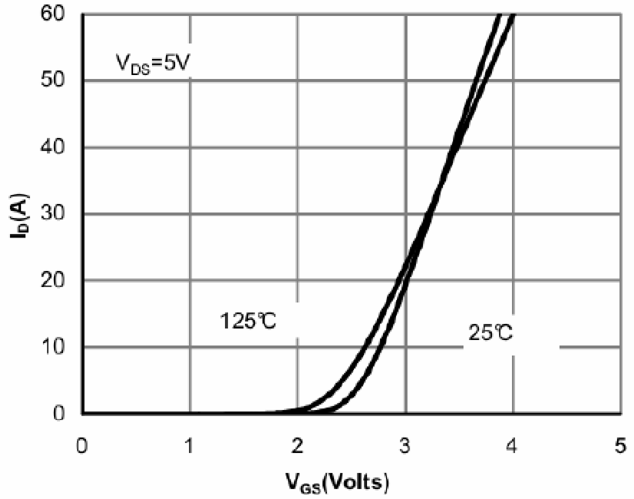


Figure 2: Transfer Characteristics (Note E)

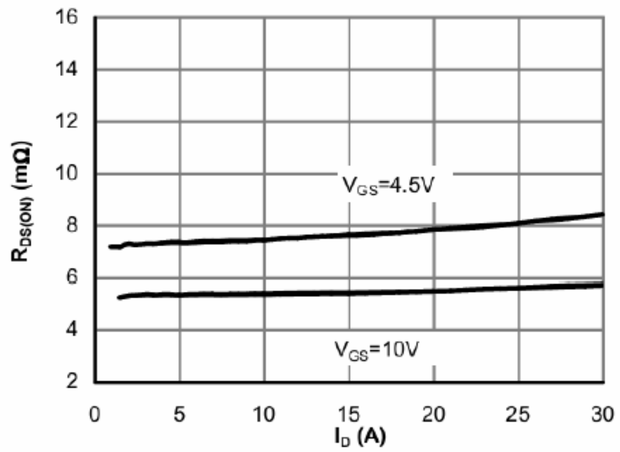


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

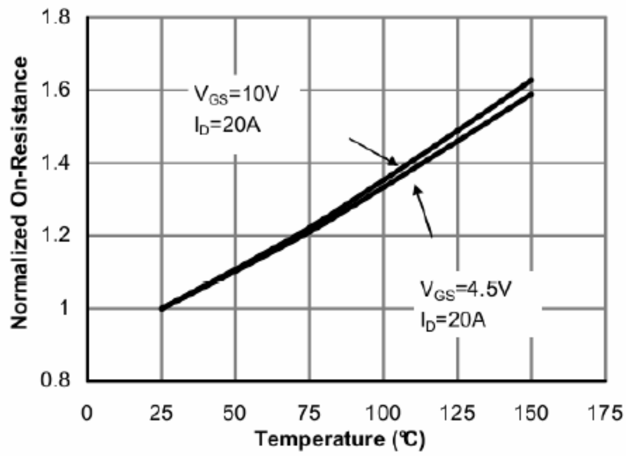


Figure 4: On-Resistance vs. Junction Temperature (Note E)

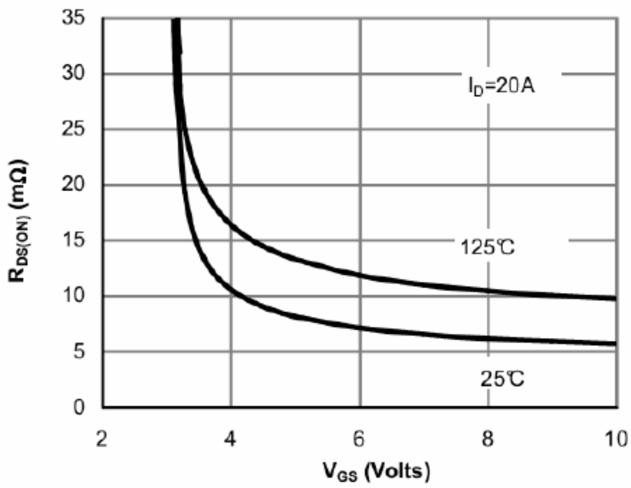


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

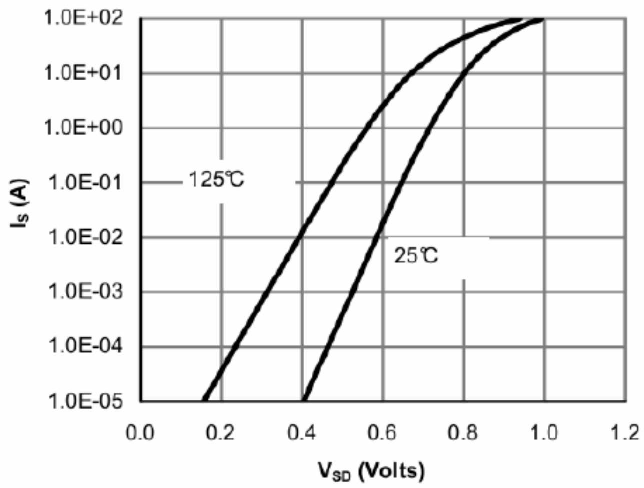


Figure 6: Body-Diode Characteristics (Note E)

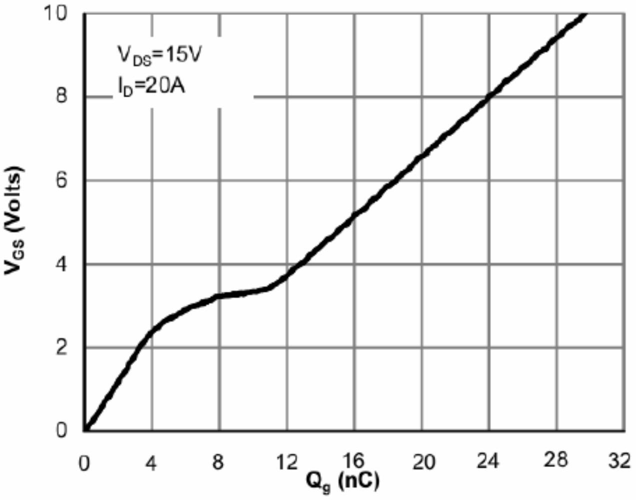


Figure 7: Gate-Charge Characteristics

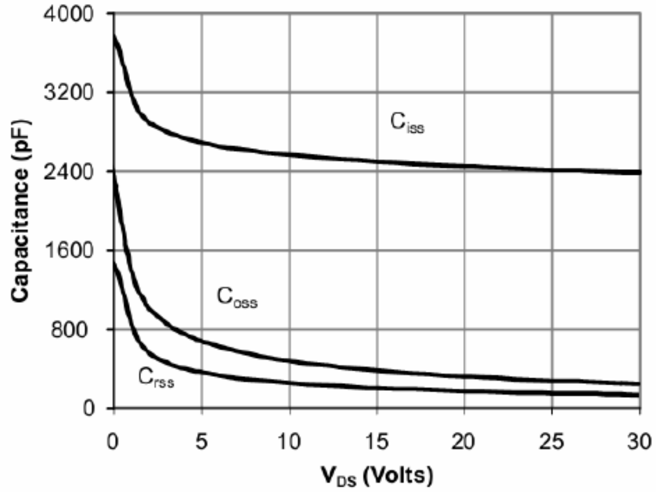


Figure 8: Capacitance Characteristics

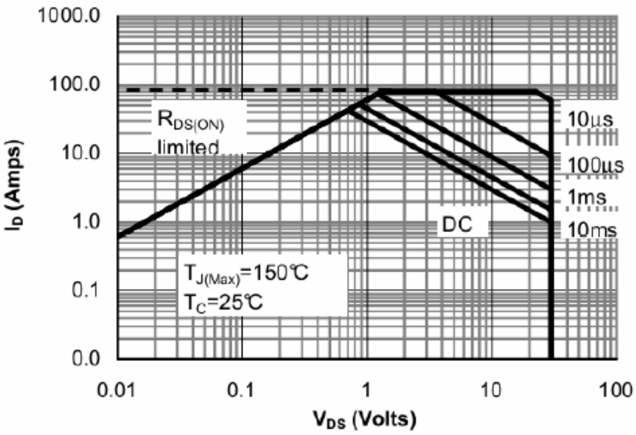


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

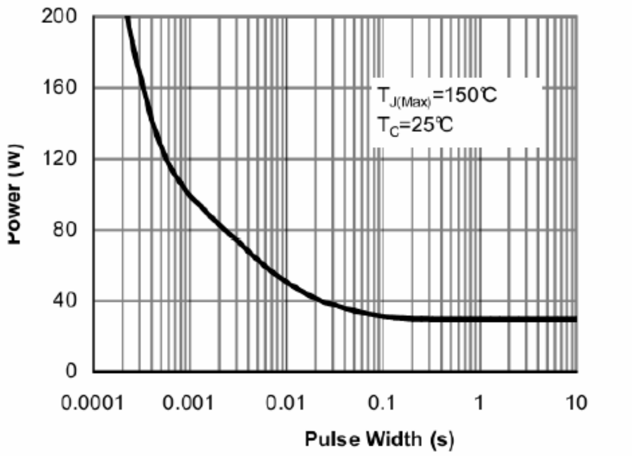


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

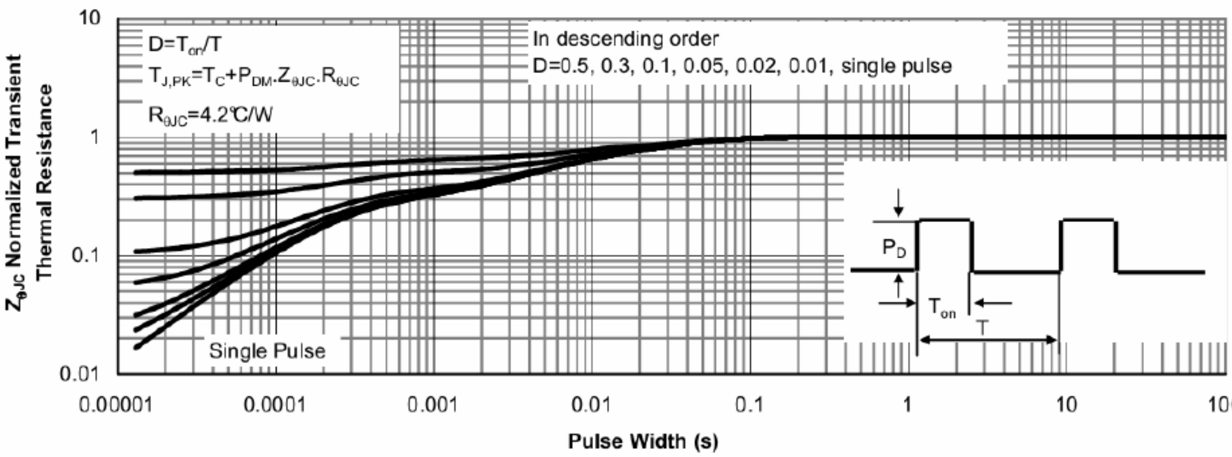


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

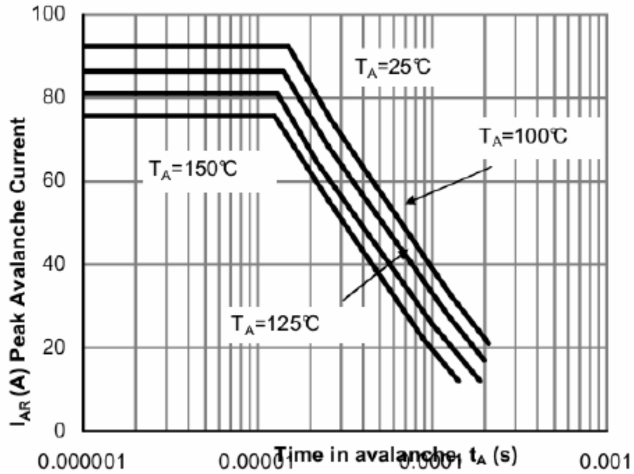


Figure12:SinglePulseAvalanche capability(Note

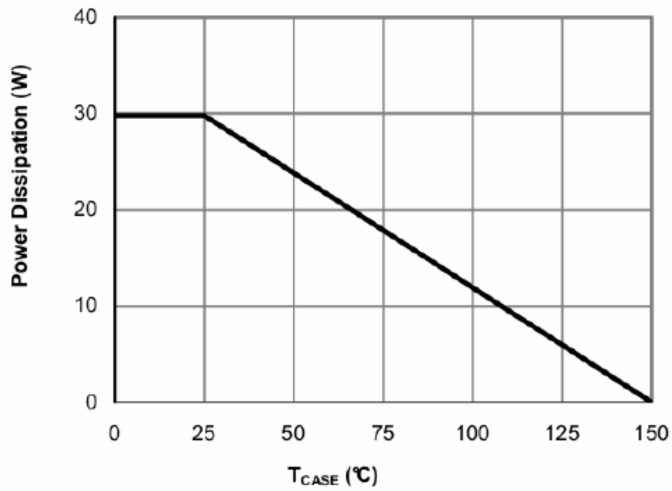


Figure 13: Power De-rating (Note F)

Typical Performance Characteristics

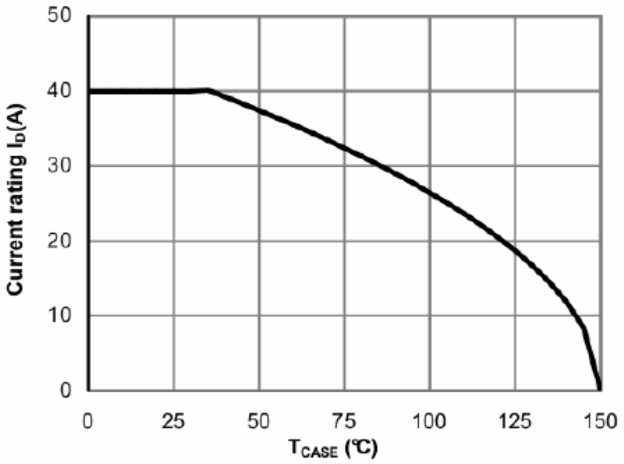


Figure 14: Current De-rating (Note F)

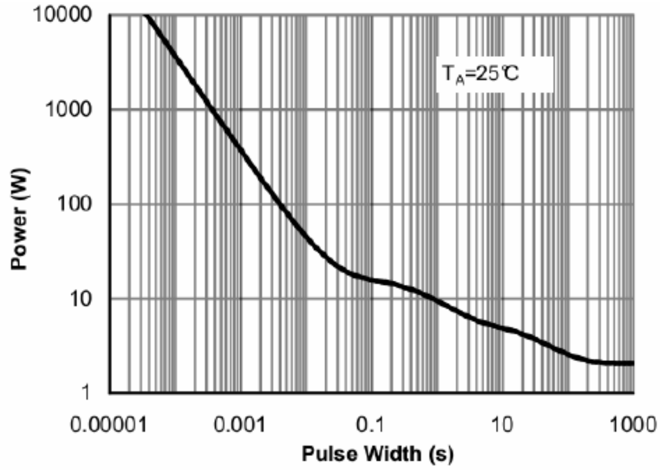


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

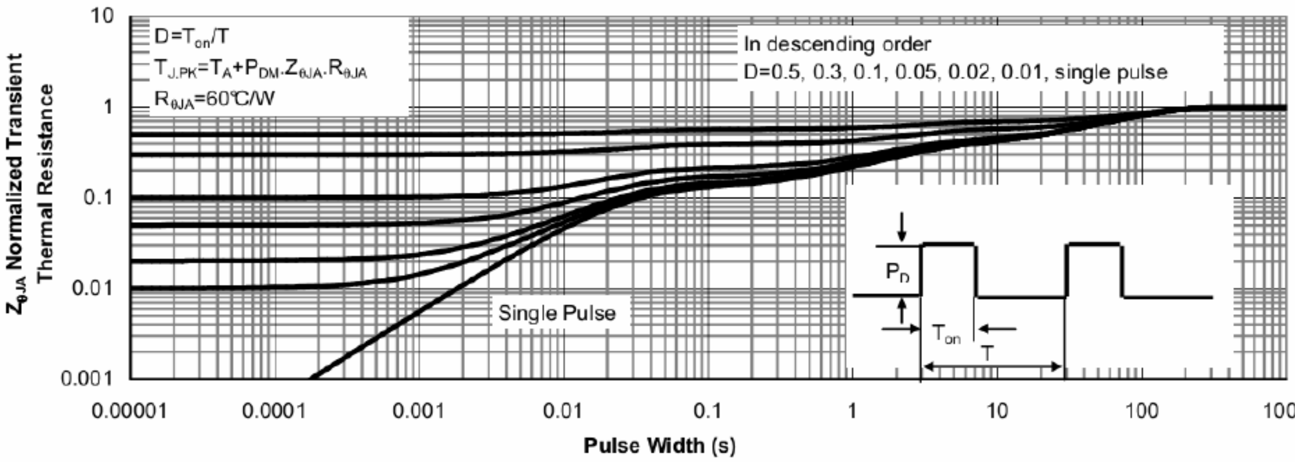
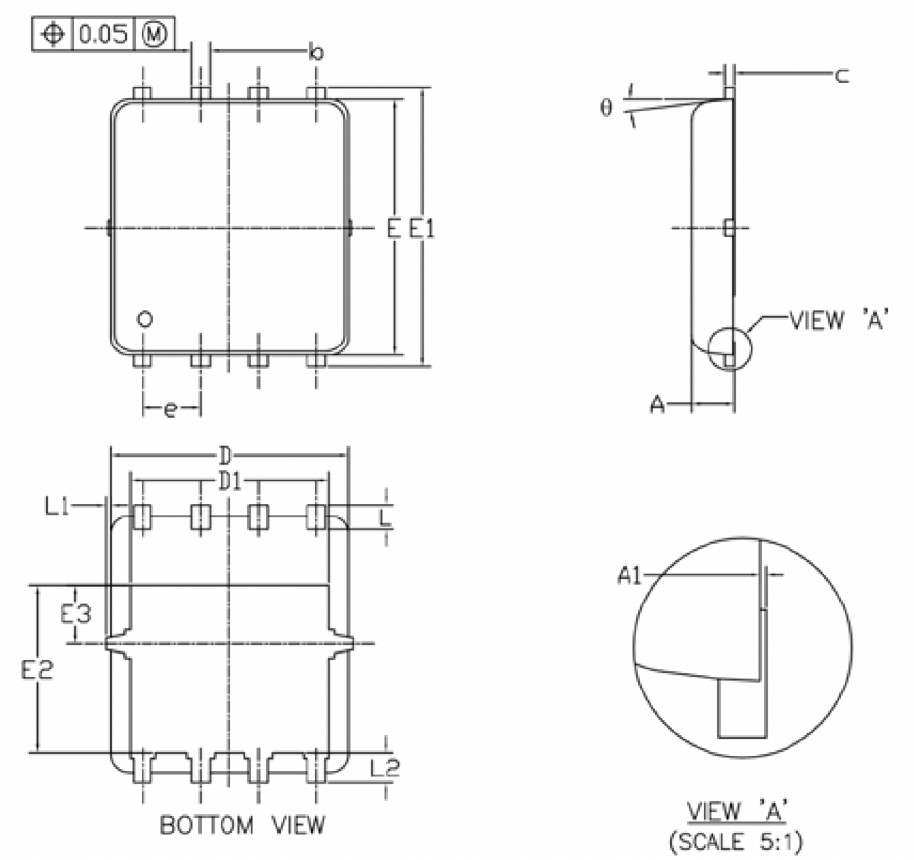


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

Packing Information

DFN5*6-8L-EP



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.85	0.95	1.00	0.033	0.037	0.039
A1	0.00	——	0.05	0.000	——	0.002
b	0.30	0.40	0.50	0.012	0.016	0.020
c	0.15	0.20	0.25	0.006	0.008	0.010
D	5.20 BSC			0.205 BSC		
D1	4.35 BSC			0.171 BSC		
E	5.55 BSC			0.219 BSC		
E1	6.05 BSC			0.238 BSC		
E2	3.625 BSC			0.143 BSC		
E3	1.275 BSC			0.050 BSC		
e	1.27 BSC			0.050 BSC		
L	0.45	0.55	0.65	0.018	0.022	0.026
L1	0	——	0.15	0	——	0.006
L2	0.68 REF			0.027 REF		
θ	0°	——	10°	0°	——	10°

Notes

ACE does not assume any responsibility for use as critical components in life support devices or systems without the express written approval of the president and general counsel of ACE Electronics Co., LTD. As sued herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and shoes failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.